ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

AD193X Codec PCB Layout Best Practices

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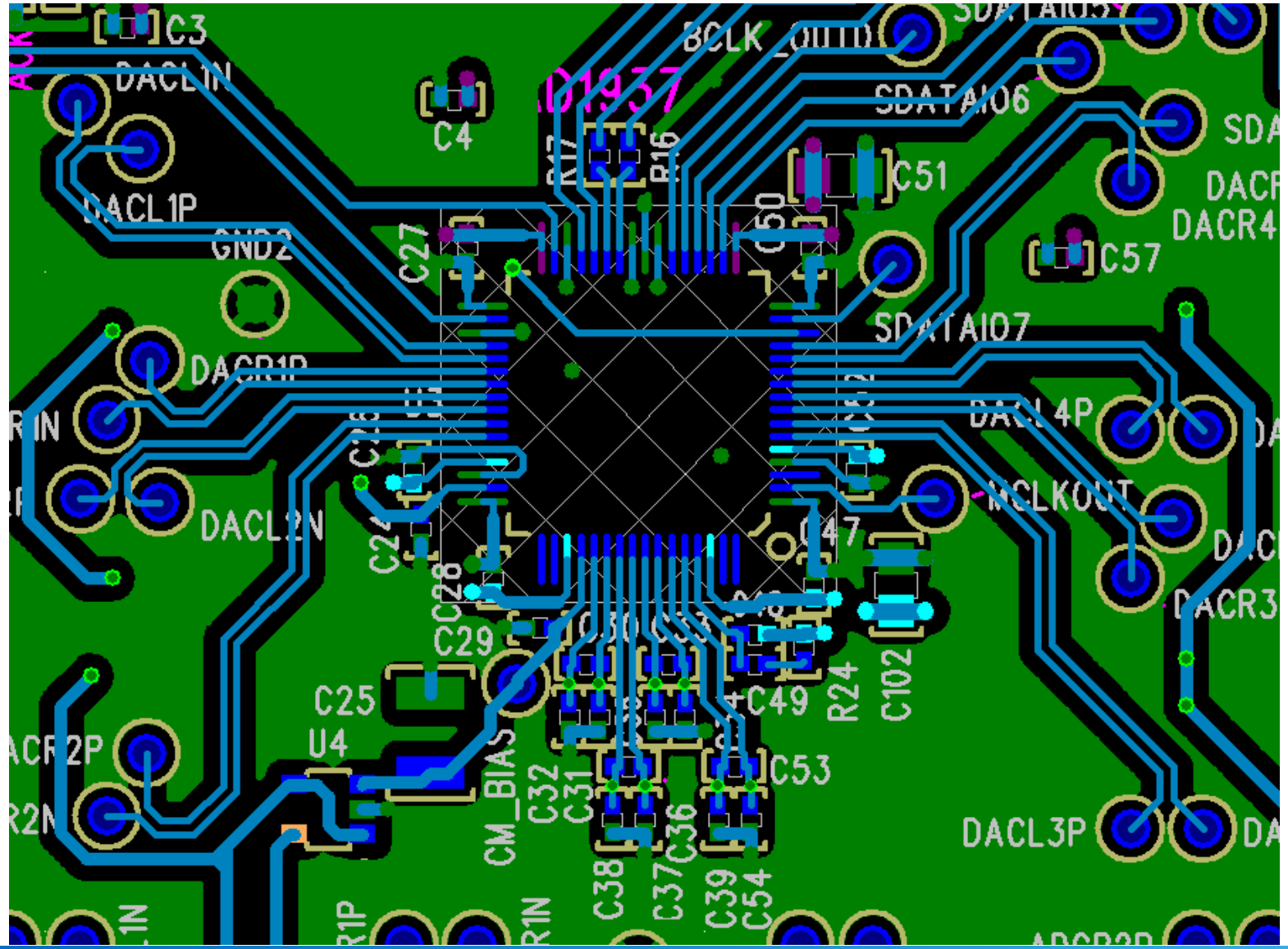
Overview

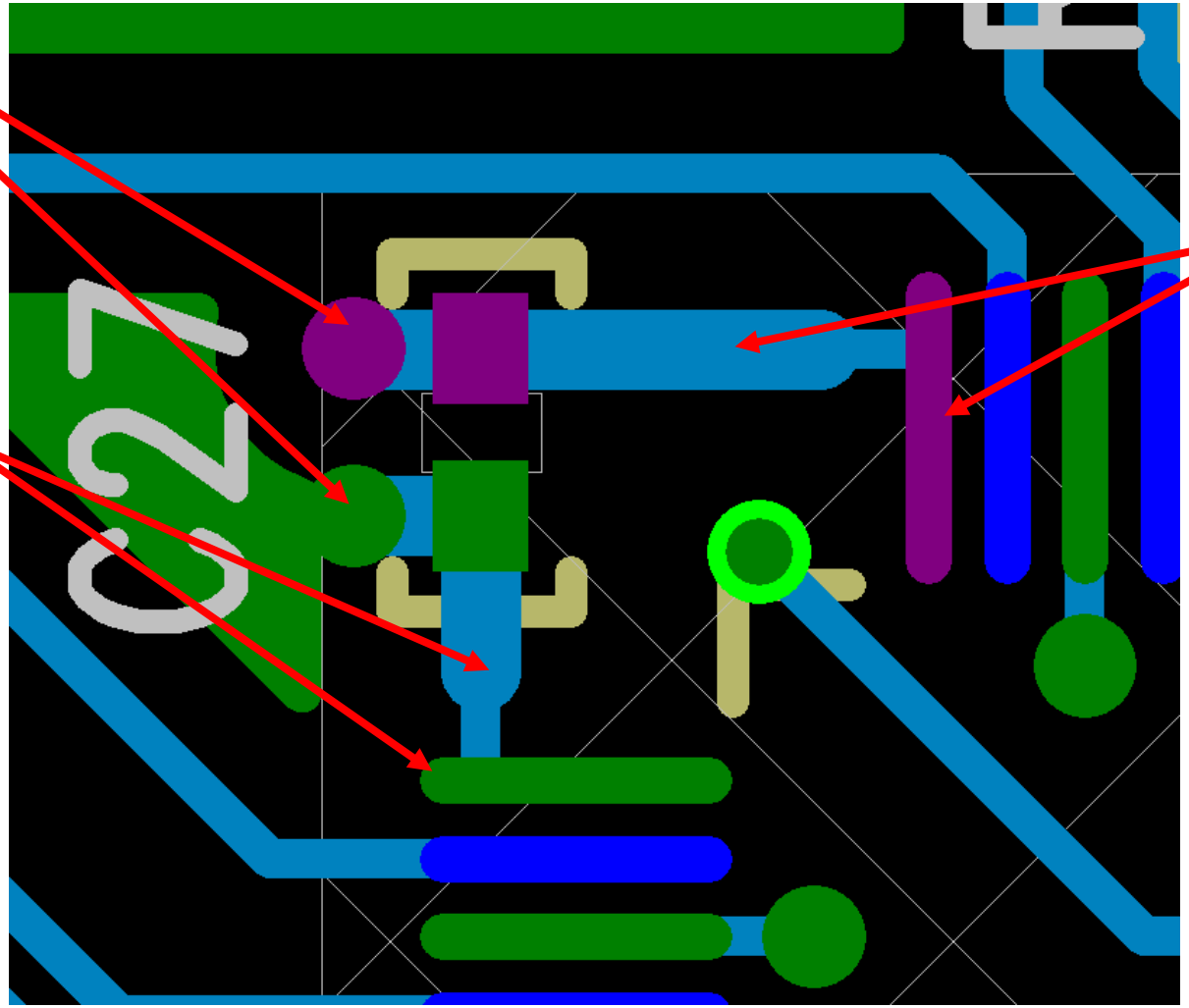
- This document details best practices for PCB layout design for the AD193x family of codecs.
- There has been several instances where poor PCB layout has caused issues with PLL locking or with simply poor analog performance such that the part does meet datasheet specifications.
- There are many other factors that will affect the analog performance. The scope of this document is to minimize the problems from poor grounding and decoupling of the codec. This will be a good step in the right direction and I have seen this solve many issues in the past.
- The concepts expressed here are valid for all components in a system and will be important for any mixed signal designs.

This example is the EVAL-ADAU1467Z which uses an AD1937 codec



Power pin decoupling Bypass Cap connections

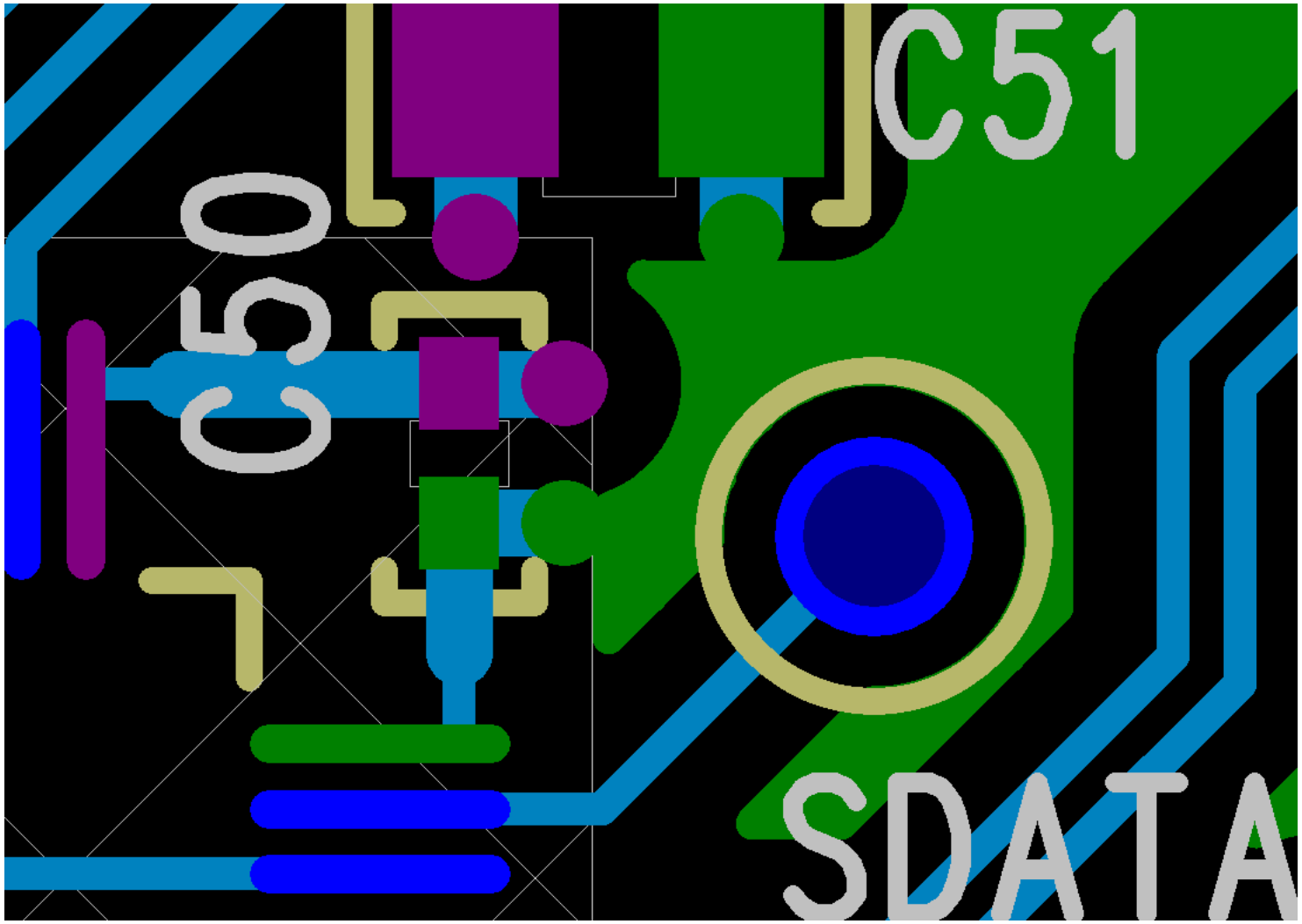
Place VIA to power and ground planes AFTER the trace passes the capacitor from the pins.



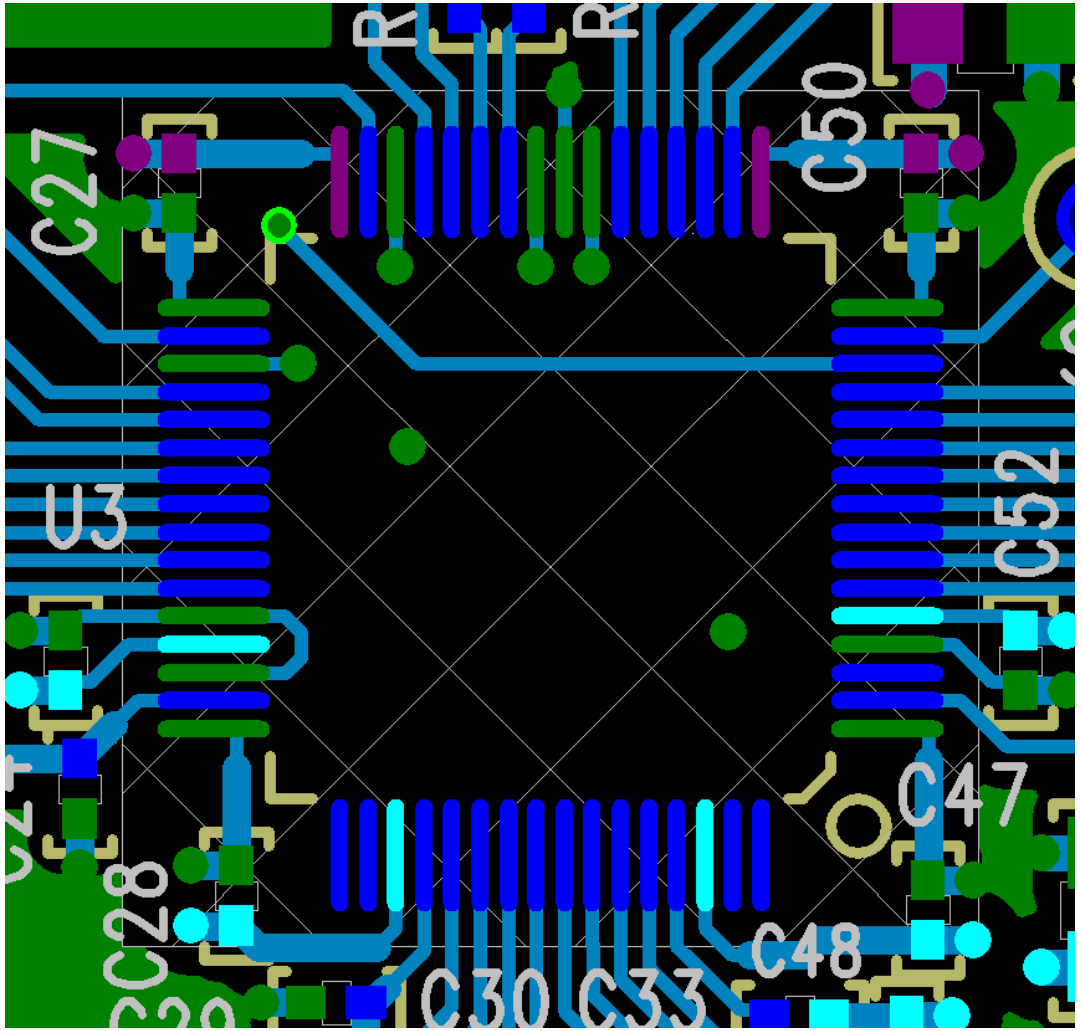
The ground pins are connected with a trace directly to the capacitor with no vias along the way. Even if the part is on the same layer, no vias and no ground fill connection until after the capacitor

Power pins are connected with a trace directly to the capacitor with no vias along the way. Even if the part is on the same layer, no vias

Another example of proper power pin decoupling cap connections to power planes and ground planes

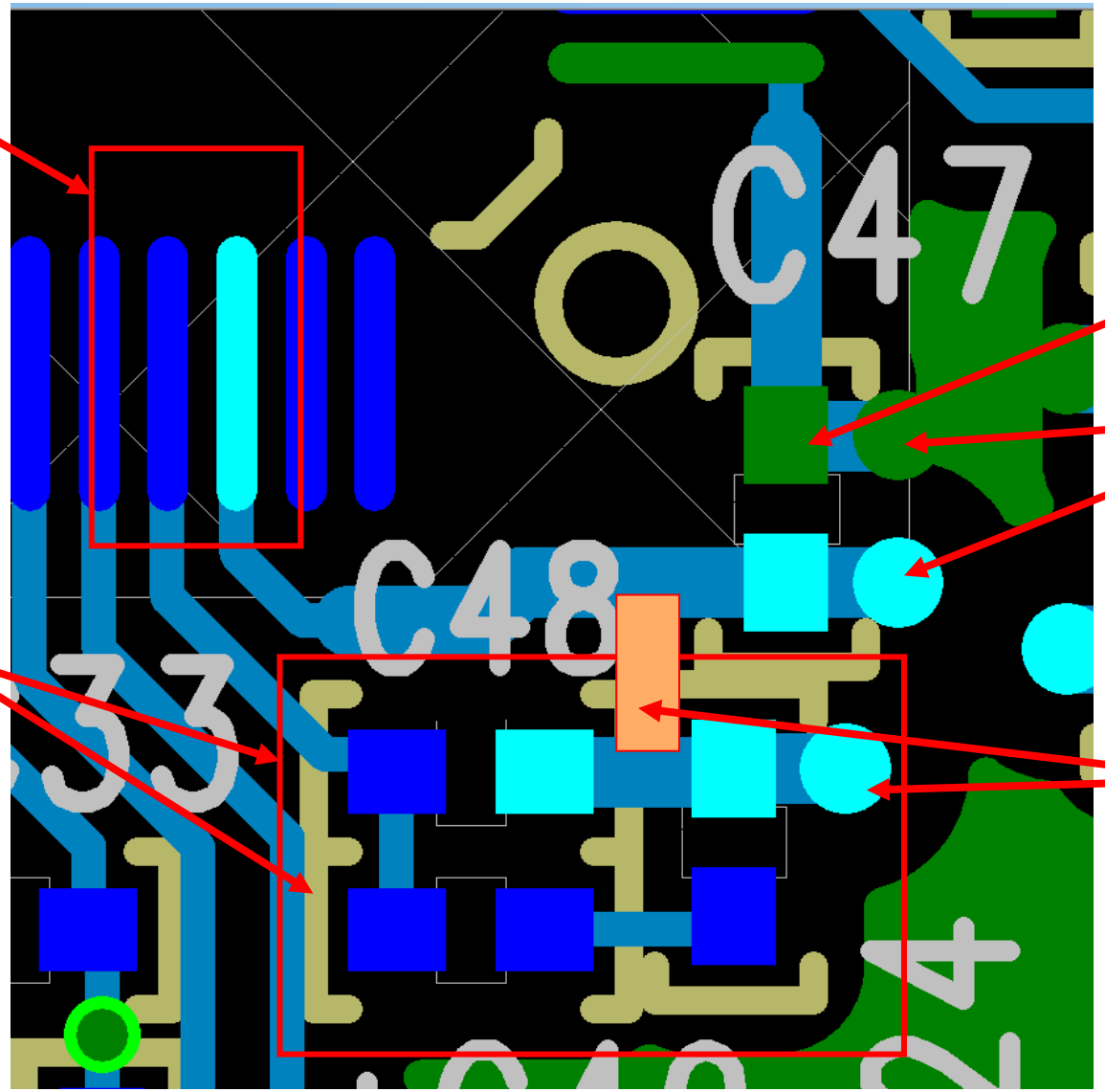


Either no ground fill under the part or if there is an EP it will have its own small ground plane with vias and prevent the PCB layout program from connecting the fill to any of the ground pins on the part.



PLL Loop Filter Connections

Loop Filter Pins.



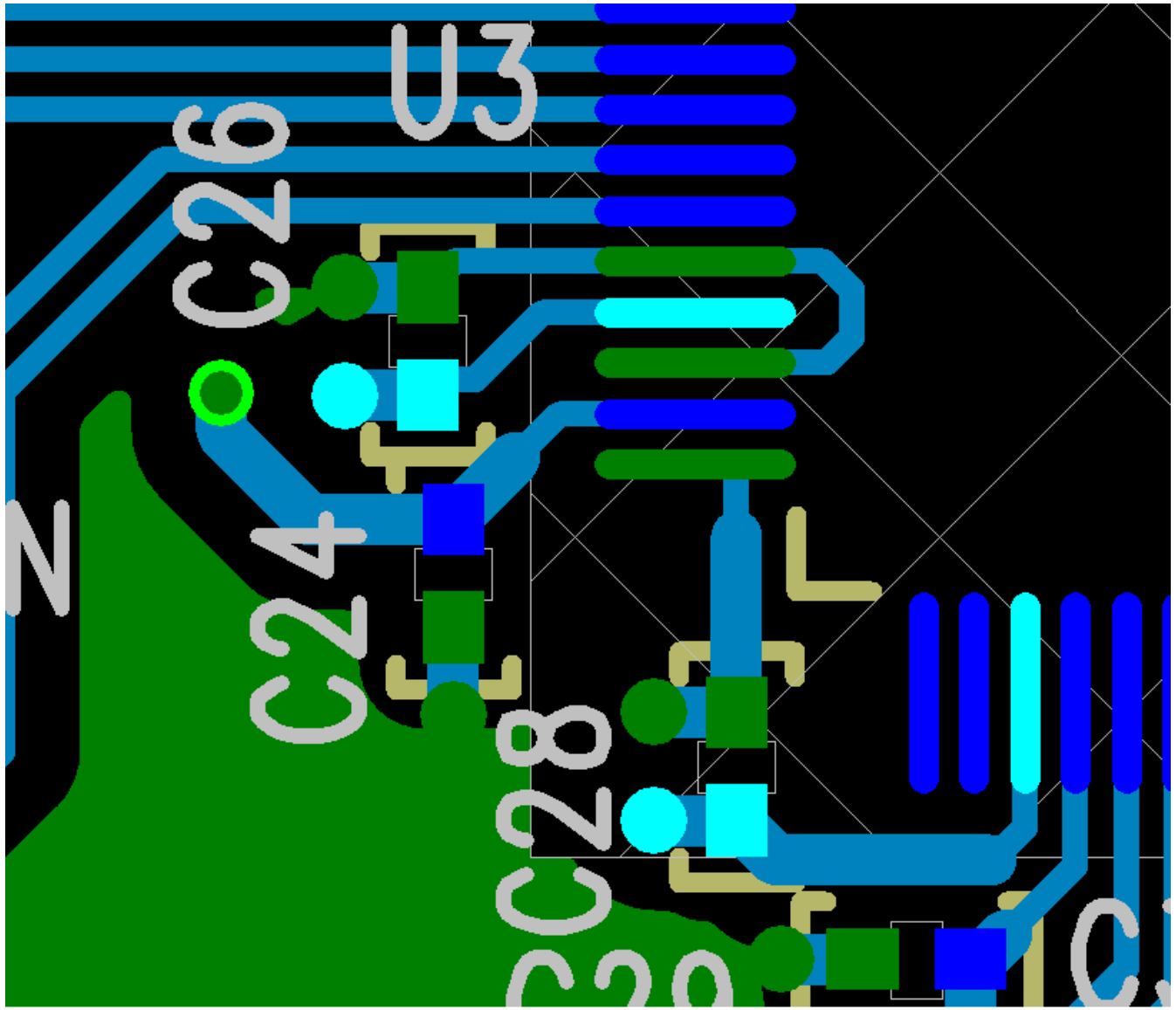
PVDD Bypass Cap

Vias to power and GND

Loop filter components MUST be on this side of the PCB and close to the part with proper connections to power and ground planes with vias after the trace from the pin to the parts.

My only complaint about this layout is that there should have been a trace here shown by the orange box and the extra via removed.

One more good example of good bypassing with this PCB design.



Overview

- I have seen these techniques used to good results for solving audio performance problems and also for solving EMI emissions problems.
- This technique for bypassing helps keep noise from within the part from getting onto the power planes and keeps any noise on the power planes from reaching the part. It is a two-way street and this allows the capacitor to do the job it is supposed to do.
- This avoids the issues with stray inductance of vias at high frequencies. The transitions of clocks and data have very high frequencies even if the clock frequency is not very high.

Thank You!

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